NEW SCALED TM DUAL-RAIL COMPUTER ARCHITECTURE

The end of the Von Neumann bottleneck

The memory (flip-flop) becomes the processor

Software/algorithms become algebraic

Deterministic AI, minimal energy consumption and safety-critical real-time

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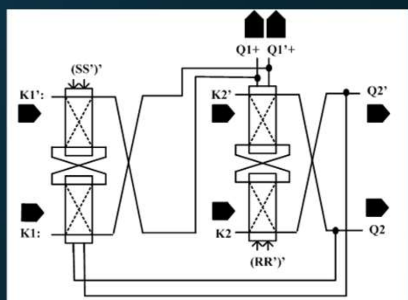
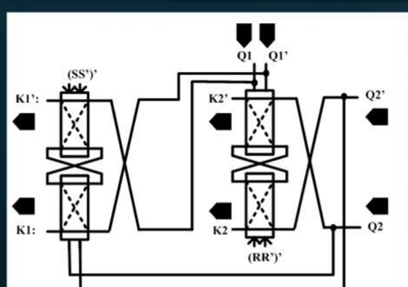
Why classical computer architectures are reaching their physical limits

- In modern processors, much of the energy and time is spent on data movement
- Memory, computing unit and control system are physically separated
- Cache hierarchies, buses, and interconnects dominate latency and power consumption
- Deterministic real-time, extreme energy efficiency and safety are structurally not achievable at the same time
- Software and algorithms are growing exponentially

TM–Dual–Rail: The memory becomes a computing unit. Software becomes algebraic

IN/OUT





OUT/IN

- Introduction of the Bidirectional Algebraic Dual-Rail Flip-Flop (BFF)
- A single physical component takes over:

  Storage

  logical operation

  Transition of state
- Switchable by swapping inputs and outputs:

  IN/OUT: sequential memory

  OUT/IN: algebraic function
- No load/store, no cache effects, no bus traffic

  Software becomes algebraic

Technical comparison: Classic vs. New TM Dual Rail

Classic:

- 20-100 cycles per state update
- High energy consumption
- Non-deterministic timing
- High system complexity

New TM Dual Rail:

- 1–2 cycles per state transition
- Energy in the pJ range (expected)
- Strictly deterministic
- Architecture is reduced complexity

Based on SPICE simulations and physical modeling

Physical validation at the transistor level

- SPICE-Simulationen at CMOS transistor level
- Dual-Rail AND-Function
- Sequential BFF (IN/OUT)
- Algebraic BFF variants (OUT/IN)
- Validated functions:
  - Set
  - Delete
  - Hold
- BFF-Core: 16 Transmission Gates (32 Transistors)

Typical Use Case: Deterministic AI in the Control Loop

- Safety-critical control loops are formal automaton models
- Classic implementation generated:
  - o Non-deterministic latencies
  - o High energy consumption
- New TM Dual Rail integrates AI decisions directly as algebraic state transitions
- Result:
  - o Deterministic real-time
  - o Minimal energy consumption
  - o Formal certifiability
- Integration as a dual-rail safety island into existing single-rail systems. Software becomes algebraic.

Current project status

- Architectural concept defined
- SPICE simulations successfully carried out
- Proven functional and temporal stability
- Patent application filed

Next steps: Patenting process, further detailed simulations, ASIC for silicon validation

Exploitation strategy

- Licensing of the TM dual-rail architecture
- Integration into:
  - Automotive Systems
  - Industrial automation
  - Energy and telecommunications infrastructure
- Focus on:
  - Safety-critical systems
  - Energy- and latency-limited applications
- Long-term market potential through new architecture class

Team & Expertise

- Over 40 years of experience in:
  - Infrastructure
  - Distributed systems
  - Safety-critical architectures
- Role:
  - Inventor
  - System and Architectural Designer
- Focus:
  - Physically based system and computer architectures

Next step

- Transition from simulation to silicon

Basis for industrial pilot projects

- Realization of an ASIC-MPV (Test Chip)
- Objective:
    - o Experimental proof of architecture
    - o Patent protection
- Wanted:
    - o Strategic industry partners
    - o Funding partners
    - o Deep Tech Investors

    Investment required : 4 - 8 million €